128-Channel Digital X-Ray Analog Front End

Data Sheet

AD8488

FEATURES

- 128 integrator channels
- Correlated double sample error correction (CDS)
  - Corrects for V_{OS} and LF noise
- Power consumption per channel
  - Normal: 11 mW
  - Low power: 4 mW
- Low input leakage current: −1.5 pA typical
- Low input referred noise (QNI): 993 e^-rms typical
- Linearity error: 0.03% typical
- Compact 17 mm × 17 mm BGA
- Selectable filter time constants
- 4 selectable input charge ranges
- 10 selectable gain ranges

APPLICATION

- High performance digital X-ray systems
- Medical X-ray
- Security (baggage scanner) systems

GENERAL DESCRIPTION

The AD8488 is a 128-channel, analog front end (AFE) designed for use in high performance digital X-ray systems. The analog channels consist of an integrator followed by a gain selectable single-ended to low impedance differential output. The analog channel converts the charge acquired by X-ray or photodiode detectors to a voltage. The channels are composed of CMOS transistors, using typical high input impedance CMOS gates. The integrators generate charge dependent voltages using a range of selectable capacitance values that accommodate a broad range of input charge values. The integrators are followed by single-ended input to differential output voltage amplifiers where offset and low frequency noise voltages are subtracted from the input voltages. A 128:1 channel differential MUX follows the buffers and drives the analog output buffer. Switch drivers and certain digital timing functions are included, and all are mounted on a 255-lead BGA substrate. Charge conversion for all 128 channels is simultaneous followed by a sequential voltage output read of the channels using a 7-bit address code. The sequence occurs twice, sampling all 128 channels. Logic control inputs, $\overline{\text{CS\_A}}$ and $\overline{\text{CS\_B}}$, select the lower and upper 64 blocks of the channel addresses.

The AD8488 is packaged in a 17 mm × 17 mm, 255-lead, RoHS-compliant ball grid array (BGA). The operating temperature range is 0°C to 85°C ambient.

FUNCTIONAL BLOCK DIAGRAM

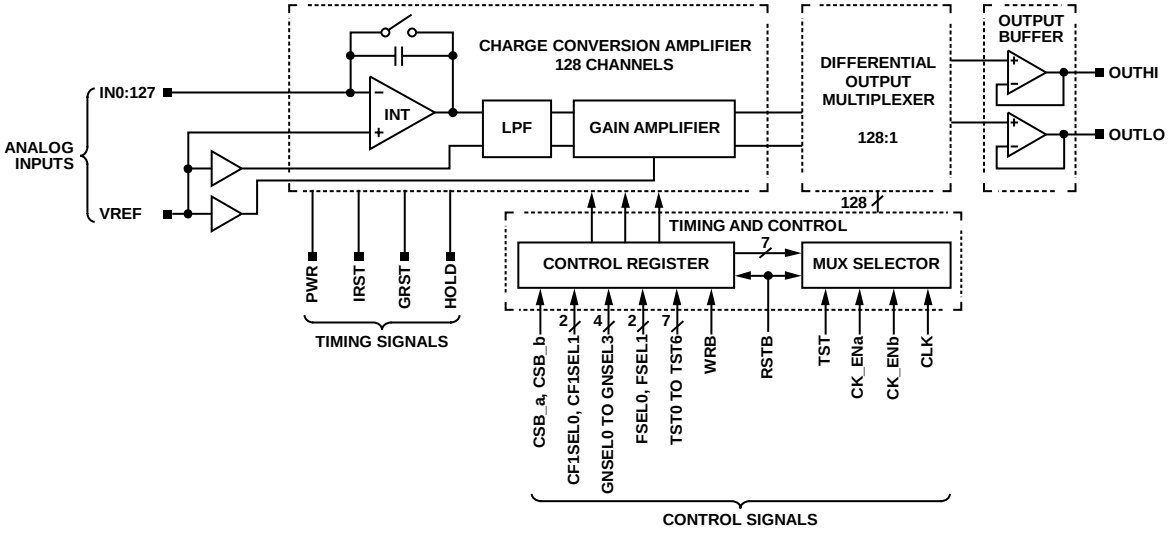

Figure 1.

Rev. A

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REVISION HISTORY

6/12—Revision A: Initial Version

SPECIFICATIONS

Default test conditions, unless otherwise specified: V_{DD} = 5 V, V_{CC} = 5 V, LPF resistor (R1) = 130 kΩ, base panel temperature = 30°C, Pin PWR = logic low, G = 1 V/V, C_H = 0.5 pF, and C_{PANEL} = 38 pF.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT LEAKAGE CURRENT		−10	−1.5	+10	pA/channel
CHARGE CONVERSION RATE[1]	See Figure 16				
	CF1 = 0.45 pF	1.7	2.3	2.9	V/pC
	CF1 = 0.9 pF	0.85	1.1	1.4	V/pC
	CF1 = 3.5 pF	0.21	0.28	0.36	V/pC
	CF1 = 7 pF	0.10	0.14	0.18	V/pC
GAIN CHARACTERISTICS					
Accuracy[2]					
CF1 = 7 pF	G = 1	0.98	1	1.02	V/V
	G = 2	1.96	2	2.04	V/V
	G = 3	2.94	3	3.06	V/V
	G = 4	3.92	4	4.08	V/V
	G = 5	4.9	5	5.1	V/V
	G = 6	5.88	6	6.12	V/V
	G = 7	6.86	7	7.14	V/V
	G = 8	7.84	8	8.16	V/V
	G = 9	8.82	9	9.18	V/V
	G = 10	9.8	10	10.2	V/V
Gain Step	Linear to 7 pC input charge		1		V/V
Error vs. Temperature[3]			0.003		%/°C
MAXIMUM INPUT CHARGE					
	CF1 = 0.45 pF		0.45		pC
	CF1 = 0.9 pF		0.9		pC
	CF1 = 3.5 pF		3.5		pC
	CF1 = 7 pF		7		pC
CLOCK					
Frequency		1		15	MHz
Rise and Fall Time				6	ns
LOGIC INTERFACE	$\overline{WR}$, CF1SELx, FSELx, GNSELx, HOLD, GRST, IRST, TSTx, CK_ENx, PWR, $\overline{CS\_A}$, $\overline{CS\_B}$				
Input High		3.25			V
Input Low				1.15	V
Leakage Current			$14.5e^{-6}$	1	µA
POWER SUPPLY					
Analog Supply					
Voltage (AV_{DD})		4.75	5	5.25	V
Quiescent Current (AI_{DD})	Pin PWR logic low	230	285	350	mA
Current in Low Power Mode	Pin PWR logic high	65	90	100	mA
Power Consumption					
Normal	Pin PWR logic low		11		mW/channel
Low Power	Pin PWR logic high		4		mW/channel
Digital Supply					
Voltage (DV_{DD})		4.75	5	5.25	V
Quiescent Current (DI_{DD})			2	10	mA
REFERENCE VOLTAGE					
VREF			2.048		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE					
OUTHIGH			2.0		V
OUTLOW			2.0		V
INPUT REFERRED NOISE[4]	CF1 = 0.9 pF, G = 10				
Normal	C_{PANEL} = 38 pF		993		e^-rms
Low Power	C_{PANEL} = 61 pF		2000		e^-rms
PANEL CAPACITANCE		0		80	pF
LINEARITY ERROR[5]	CF1 = 0.9 pF, G = 5				
Normal			0.03 + 1		% + LSB
Low Power			0.2 + 8.2		% + LSB
OPERATING TEMPERATURE	Ambient, normal and low power	0		85	°C

[1] Defined as the output voltage divided by the input charge (number of electrons in this case) with the gain amp setting (G = 1). This includes the gain error of the gain amp.
[2] Each gain at G = 2, G = 4, G = 8, and G = 10 is calculated as the ratio of each output voltage to that at G = 1. Each measurement corresponds to the selection of each gain setting capacitor.
[3] Gain deviation over temperature.
[4] The output noise voltage is measured and converted into the input referred noise electrons.
[5] It is defined as the deviation from a best fit line, including the origin. The output voltage is measured with five different input conditions.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply (AV_{DD}, DV_{DD})	5.5 V
Charge Input IN0 to IN127	−0.3 V to VREF + 0.3 V
Reference (VREF, VREF_ESD)	5.5 V
Logic Inputs	−0.3 V to +5.5 V
Maximum Junction Temperature	125°C
Storage Temperature Range	−30°C to +150°C
Input Charge to Integrator Channels	20 pC

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Ψ_{JB} is the junction-to-board thermal characterization parameter with a unit of °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path, as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL CHARACTERIZATION

Table 3. Thermal Resistance—Normal Operation (1.4 W)

Airflow Velocity (m/sec)	Ambient	θ_{JA}	Ψ_{JT}	Ψ_{JB}	θ_{JC}	Unit
0	85°C	18.6	0.20	8.3	4.4	°C/W
	50°C	19.7	0.17	8.3	4.4	°C/W
	25°C	20.6	0.16	8.3	4.4	°C/W
1	85°C	15.8	0.32	8.2	4.4	°C/W
	50°C	16.1	0.30	8.2	4.4	°C/W
	25°C	16.4	0.29	8.2	4.4	°C/W
3	85°C	13.8	0.54	7.7	4.4	°C/W
	50°C	14.0	0.53	7.7	4.4	°C/W
	25°C	14.2	0.52	7.7	4.4	°C/W

Table 4. Thermal Resistance—Low Power Operation (0.5 W)

Airflow Velocity (m/sec)	Ambient	θ_{JA}	Ψ_{JT}	Ψ_{JB}	θ_{JC}	Unit
0	85°C	19.0	0.19	8.3	4.4	°C/W
	50°C	20.2	0.16	8.3	4.4	°C/W
	25°C	21.2	0.15	8.3	4.4	°C/W
1	85°C	15.7	0.31	8.1	4.4	°C/W
	50°C	16.2	0.29	8.1	4.4	°C/W
	25°C	16.4	0.28	8.1	4.4	°C/W
3	85°C	13.8	0.54	7.8	4.4	°C/W
	50°C	14.1	0.52	7.8	4.4	°C/W
	25°C	14.2	0.51	7.8	4.4	°C/W

Note that the thermal numbers are simulated per JEDEC JESD51-9 on a 4-layer printed circuit board size = 101.5 mm × 114.5 mm.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

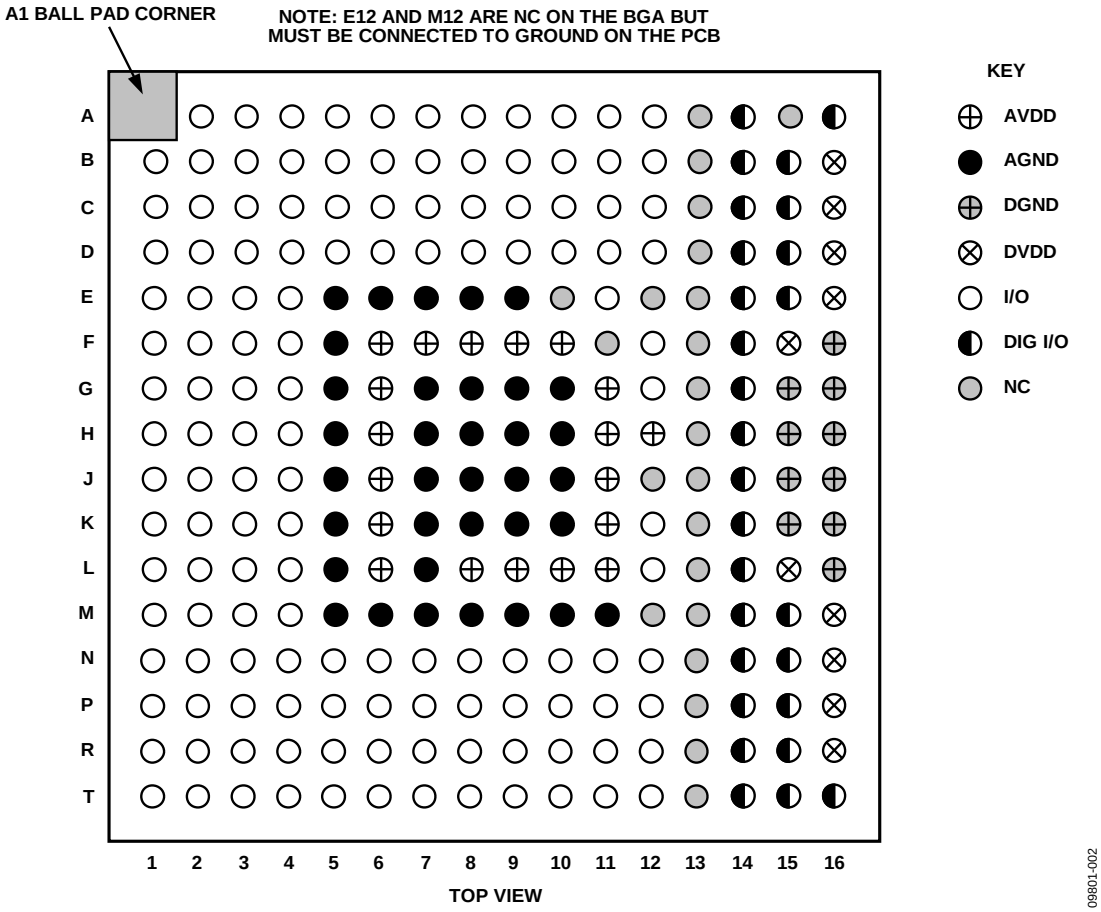


Figure 2. 255-Ball CSP_BGA Ball Configuration (Top View)

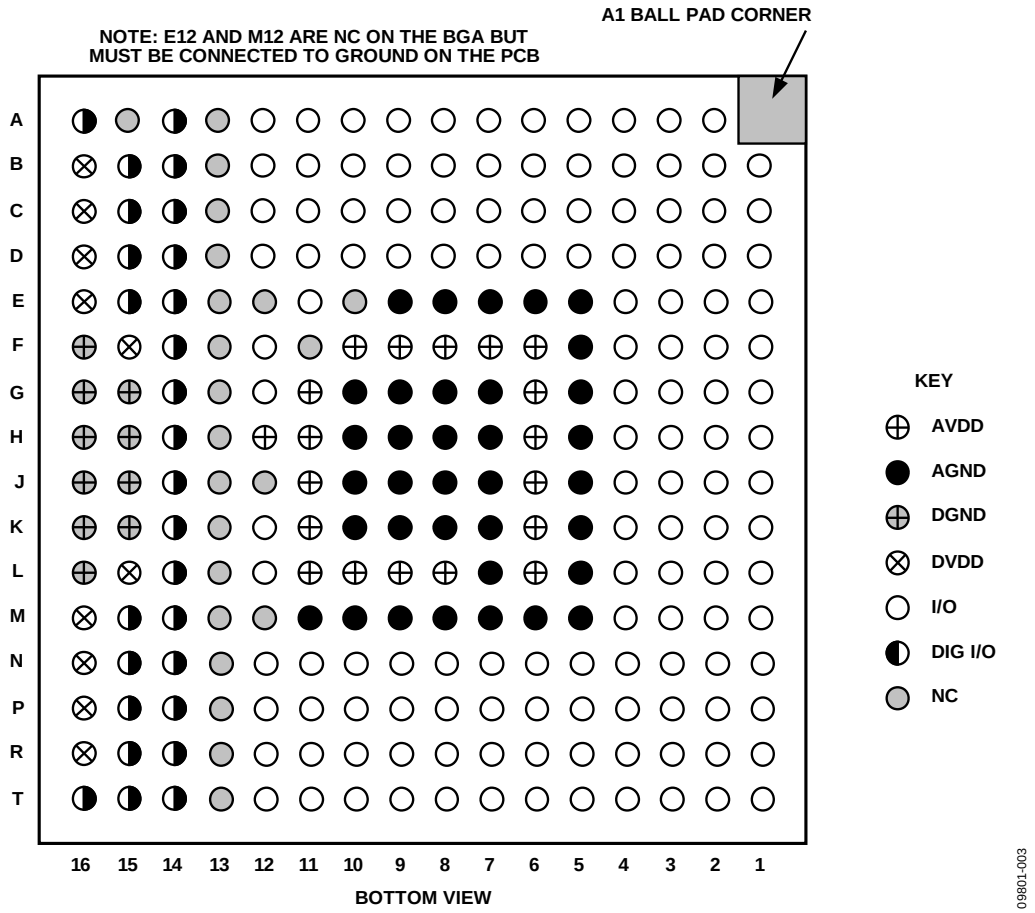


Figure 3. 255-Ball CSP_BGA Ball Configuration (Bottom View)

Table 5. Pin Function Descriptions

Mnemonic	Pin No.	I/O	Description
AGND	See Table 6 and Table 7	O	Analog Power Ground (0 V).
AVDD	F6, F7, F8, F9, F10, G6, G11, H6, H11, H12, J6, J11, K6, K11, L6, L8, L9, L10, L11	I	Analog Supply Voltage (5 V).
CLK	D15	I	Clock for Mux Operation.
CK_ENa	E14	I	Clock Gate for Channel 0 to Channel 63.
CK_ENb	F14	I	Clock Gate for Channel 64 to Channel 127.
$\overline{\text{CS\_A}}$	N14	I	Logic Level to Enable Channel 0 to Channel 63.
$\overline{\text{CS\_B}}$	M15	I	Logic Level to Enable Channel 64 to Channel 127.
CF1SEL0, CF1SEL1	B15, C15	I	Binary Coded Logic Pins to Select One of Four Values of Integrator Capacitor CF1 (see Table 9).
DGND	F16, G15, G16, H15, H16, J15, J16, K15, K16, L16	O	Digital Ground (0 V).
DVDD	B16, C16, D16, E16, F15, L15, M16, N16, P16, R16	I	Power Supply for Digital Circuit (5 V).
FSEL0, FSEL1	R14, T14	I	Filter Time Constant Select (see Table 10).
GNSEL0 to GNSEL3	A14, B14, C14, D14	I	Gain Select for the Gain Amp. Select one of four hold capacitors. The four values are arranged in one of ten parallel options to establish ten gain values (see Table 11).
GRST	H14	I	Gain Amp Reset. Closes the switch across Integrator Capacitor CF2 setting the output of the gain amplifier to zero.
HOLD	T16	I	Gain Amp Hold. Connect the hold capacitor to the signal chain.

Mnemonic	Pin No.	I/O	Description
IN0 to IN127	See Table 6 and Table 7	I	Analog Inputs.
IRST	E15	I	Integrator Reset. Closes a switch across the integration capacitor, CF1, to set the output to zero.
NC	A13, A15, B13, C13, D13, E10, E12, E13, F11, F13, G13, H13, J12, J13, K13, L13, M12, M13, N13, P13, R13, T13		No connect. Connect these pins to GND on the PCB.
OUTLOW	F12	O	Inverting Analog Output (Negative) of the Differential Output.
OUTHIGH	G12	O	Noninverting Analog Output (Positive) of the Differential Output.
PWR	P14	I	Normal state is logic low; reduces analog bias current by approximately 80% when high.
$\overline{\text{RST}}$	A16	I	Reset Gray Mode Counter for Mux.
TST_MODE	J14	I	Test Mode Enable. This control line is used together with the TST0 to TST6 address bits to test or debug a system by continuously selecting a channel.
TST0 to TST6	T15, R15, P15, N15, M14, L14, K14	I	Channel Address Select Bits When in Test Mode (see Table 8).
VREF	L12	I	Reference Input for Analog Circuit (2.048 V).
VREF_ESD	K12	I	ESD Reference. Connect to VREF (2.048 V).
$\overline{\text{WR}}$	G14	I	Write Digital Instruction Word to the AFE.

SIGNAL MNEMONICS

Table 6. 255-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A2	IN108	C14	GNSEL1	F10	AVDD	J6	AVDD	M2	IN50	P14	PWR
A3	IN107	C15	CF1SEL0	F11	NC	J7	AGND	M3	IN49	P15	TST2
A4	IN106	C16	DVDD	F12	OUTLOW	J8	AGND	M4	IN48	P16	DVDD
A5	IN80	D1	IN91	F13	NC	J9	AGND	M5	AGND	R1	IN25
A6	IN84	D2	IN90	F14	CK_ENb	J10	AGND	M6	AGND	R2	IN26
A7	IN110	D3	IN89	F15	DVDD	J11	AVDD	M7	AGND	R3	IN27
A8	IN111	D4	IN88	F16	DGND	J12	NC	M8	AGND	R4	IN28
A9	IN112	D5	IN87	G1	IN73	J13	NC	M9	AGND	R5	IN29
A10	IN115	D6	IN86	G2	IN72	J14	TST_MODE	M10	AGND	R6	IN30
A11	IN119	D7	IN85	G3	IN71	J15	DGND	M11	AGND	R7	IN23
A12	IN124	D8	IN83	G4	IN70	J16	DGND	M12	NC	R8	IN22
A13	NC	D9	IN118	G5	AGND	K1	IN59	M13	NC	R9	IN15
A14	GNSEL3	D10	IN109	G6	AVDD	K2	IN58	M14	TST4	R10	IN11
A15	NC	D11	IN123	G7	AGND	K3	IN57	M15	$\overline{CS\_B}$	R11	IN5
A16	$\overline{RST}$	D12	IN126	G8	AGND	K4	IN56	M16	DVDD	R12	IN6
B1	IN103	D13	NC	G9	AGND	K5	AGND	N1	IN41	R13	NC
B2	IN102	D14	GNSEL0	G10	AGND	K6	AVDD	N2	IN46	R14	FSEL0
B3	IN101	D15	CLK	G11	AVDD	K7	AGND	N3	IN45	R15	TST1
B4	IN100	D16	DVDD	G12	OUTHIGH	K8	AGND	N4	IN44	R16	DVDD
B5	IN99	E1	IN75	G13	NC	K9	AGND	N5	IN43	T1	IN19
B6	IN98	E2	IN69	G14	$\overline{WR}$	K10	AGND	N6	IN42	T2	IN18
B7	IN105	E3	IN68	G15	DGND	K11	AVDD	N7	IN51	T3	IN17
B8	IN104	E4	IN82	G16	DGND	K12	VREF_ESD	N8	IN32	T4	IN8
B9	IN113	E5	AGND	H1	IN67	K13	NC	N9	IN40	T5	IN16
B10	IN116	E6	AGND	H2	IN66	K14	TST6	N10	IN33	T6	IN20
B11	IN120	E7	AGND	H3	IN65	K15	DGND	N11	IN0	T7	IN21
B12	IN125	E8	AGND	H4	IN64	K16	DGND	N12	IN9	T8	IN13
B13	NC	E9	AGND	H5	AGND	L1	IN55	N13	NC	T9	IN10
B14	GNSEL2	E10	NC	H6	AVDD	L2	IN54	N14	$\overline{CS\_A}$	T10	IN4
B15	CF1SEL1	E11	IN122	H7	AGND	L3	IN53	N15	TST3	T11	IN2
B16	DVDD	E12	NC	H8	AGND	L4	IN52	N16	DVDD	T12	IN3
C1	IN97	E13	NC	H9	AGND	L5	AGND	P1	IN31	T13	NC
C2	IN96	E14	CK_ENa	H10	AGND	L6	AVDD	P2	IN39	T14	FSEL1
C3	IN95	E15	IRST	H11	AVDD	L7	AGND	P3	IN37	T15	TST0
C4	IN94	E16	DVDD	H12	AVDD	L8	AVDD	P4	IN38	T16	HOLD
C5	IN93	F1	IN79	H13	NC	L9	AVDD	P5	IN36		
C6	IN92	F2	IN78	H14	GRST	L10	AVDD	P6	IN35		
C7	IN81	F3	IN77	H15	DGND	L11	AVDD	P7	IN34		
C8	IN74	F4	IN76	H16	DGND	L12	VREF	P8	IN24		
C9	IN114	F5	AGND	J1	IN63	L13	NC	P9	IN14		
C10	IN117	F6	AVDD	J2	IN62	L14	TST5	P10	IN12		
C11	IN121	F7	AVDD	J3	IN61	L15	DVDD	P11	IN1		
C12	IN127	F8	AVDD	J4	IN60	L16	DGND	P12	IN7		
C13	NC	F9	AVDD	J5	AGND	M1	IN47	P13	NC		

Table 7. 255-Ball CSP_BGA Ball Assignment (Alphabetically by Signal)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
AGND	E5	AVDD	H12	HOLD	T16	IN43	N5	IN87	D5	NC	B13
AGND	E6	AVDD	J6	IN0	N11	IN44	N4	IN88	D4	NC	C13
AGND	E7	AVDD	J11	IN1	P11	IN45	N3	IN89	D3	NC	D13
AGND	E8	AVDD	K6	IN2	T11	IN46	N2	IN90	D2	NC	E10
AGND	E9	AVDD	K11	IN3	T12	IN47	M1	IN91	D1	NC	E12
AGND	F5	AVDD	L6	IN4	T10	IN48	M4	IN92	C6	NC	E13
AGND	G5	AVDD	L8	IN5	R11	IN49	M3	IN93	C5	NC	F11
AGND	G7	AVDD	L9	IN6	R12	IN50	M2	IN94	C4	NC	F13
AGND	G8	AVDD	L10	IN7	P12	IN51	N7	IN95	C3	NC	G13
AGND	G9	AVDD	L11	IN8	T4	IN52	L4	IN96	C2	NC	H13
AGND	G10	CLK	D15	IN9	N12	IN53	L3	IN97	C1	NC	J12
AGND	H5	CK_ENa	E14	IN10	T9	IN54	L2	IN98	B6	NC	J13
AGND	H7	CK_ENb	F14	IN11	R10	IN55	L1	IN99	B5	NC	K13
AGND	H8	$\overline{\text{CS\_A}}$	N14	IN12	P10	IN56	K4	IN100	B4	NC	L13
AGND	H9	$\overline{\text{CS\_B}}$	M15	IN13	T8	IN57	K3	IN101	B3	NC	M12
AGND	H10	CF1SEL0	C15	IN14	P9	IN58	K2	IN102	B2	NC	M13
AGND	J5	CF1SEL1	B15	IN15	R9	IN59	K1	IN103	B1	NC	N13
AGND	J7	DGND	F16	IN16	T5	IN60	J4	IN104	B8	NC	P13
AGND	J8	DGND	G15	IN17	T3	IN61	J3	IN105	B7	NC	R13
AGND	J9	DGND	G16	IN18	T2	IN62	J2	IN106	A4	NC	T13
AGND	J10	DGND	H15	IN19	T1	IN63	J1	IN107	A3	OUTLOW	F12
AGND	K5	DGND	H16	IN20	T6	IN64	H4	IN108	A2	OUTHIGH	G12
AGND	K7	DGND	J15	IN21	T7	IN65	H3	IN109	D10	PWR	P14
AGND	K8	DGND	J16	IN22	R8	IN66	H2	IN110	A7	$\overline{\text{RST}}$	A16
AGND	K9	DGND	K15	IN23	R7	IN67	H1	IN111	A8	TST_MODE	J14
AGND	K10	DGND	K16	IN24	P8	IN68	E3	IN112	A9	TST0	T15
AGND	L5	DGND	L16	IN25	R1	IN69	E2	IN113	B9	TST1	R15
AGND	L7	DVDD	B16	IN26	R2	IN70	G4	IN114	C9	TST2	P15
AGND	M5	DVDD	C16	IN27	R3	IN71	G3	IN115	A10	TST3	N15
AGND	M6	DVDD	D16	IN28	R4	IN72	G2	IN116	B10	TST4	M14
AGND	M7	DVDD	E16	IN29	R5	IN73	G1	IN117	C10	TST5	L14
AGND	M8	DVDD	F15	IN30	R6	IN74	C8	IN118	D9	TST6	K14
AGND	M9	DVDD	L15	IN31	P1	IN75	E1	IN119	A11	VREF	L12
AGND	M10	DVDD	M16	IN32	N8	IN76	F4	IN120	B11	VREF_ESD	K12
AGND	M11	DVDD	N16	IN33	N10	IN77	F3	IN121	C11	$\overline{\text{WR}}$	G14
AVDD	F6	DVDD	P16	IN34	P7	IN78	F2	IN122	E11		
AVDD	F7	DVDD	R16	IN35	P6	IN79	F1	IN123	D11		
AVDD	F8	FSEL0	R14	IN36	P5	IN80	A5	IN124	A12		
AVDD	F9	FSEL1	T14	IN37	P3	IN81	C7	IN125	B12		
AVDD	F10	GRST	H14	IN38	P4	IN82	E4	IN126	D12		
AVDD	G6	GNSEL0	D14	IN39	P2	IN83	D8	IN127	C12		
AVDD	G11	GNSEL1	C14	IN40	N9	IN84	A6	IRST	E15		
AVDD	H6	GNSEL2	B14	IN41	N1	IN85	D7	NC	A13		
AVDD	H11	GNSEL3	A14	IN42	N6	IN86	D6	NC	A15		

TYPICAL PERFORMANCE CHARACTERISTICS

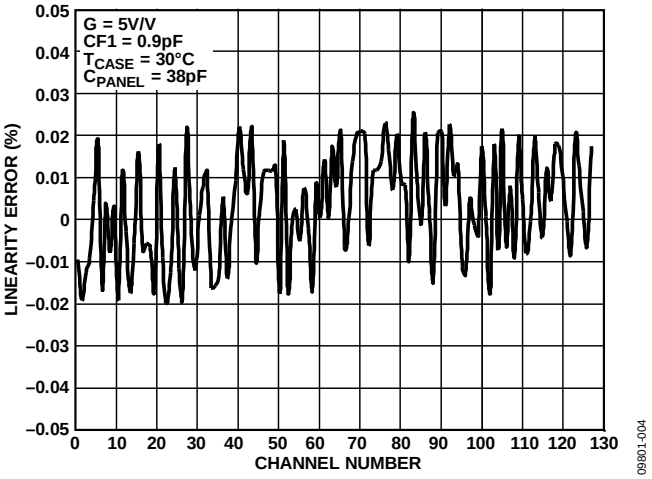


Figure 4. Linearity Error vs. Channel

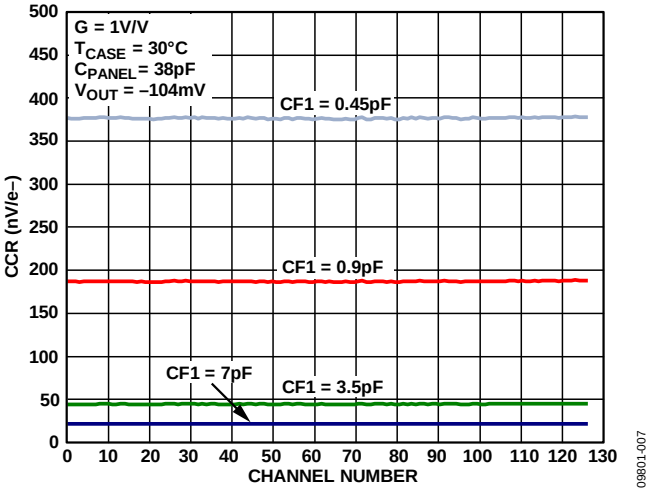


Figure 7. CCR vs. Channel for Four Values of CF1

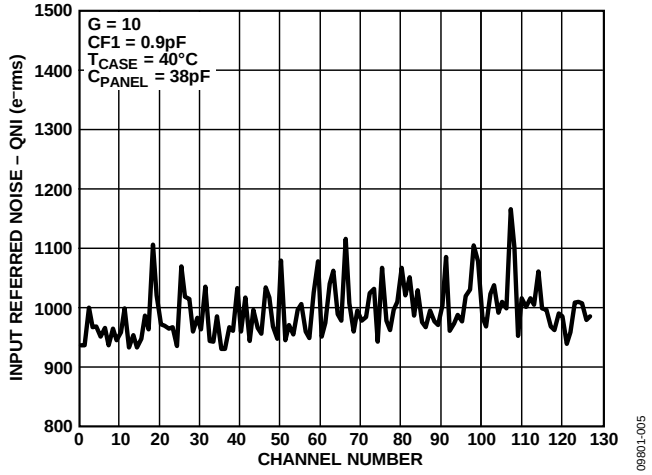


Figure 5. Input Referred Noise (QNI) vs. Channel, C_{PANEL} = 38 pF, T_{CASE} = 40°C

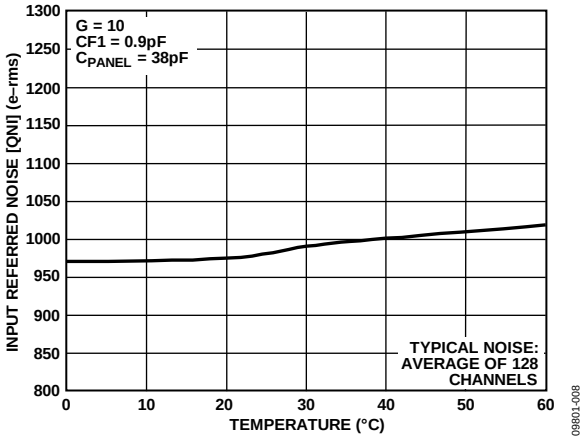


Figure 8. Input Referred Noise (QNI) vs. Temperature

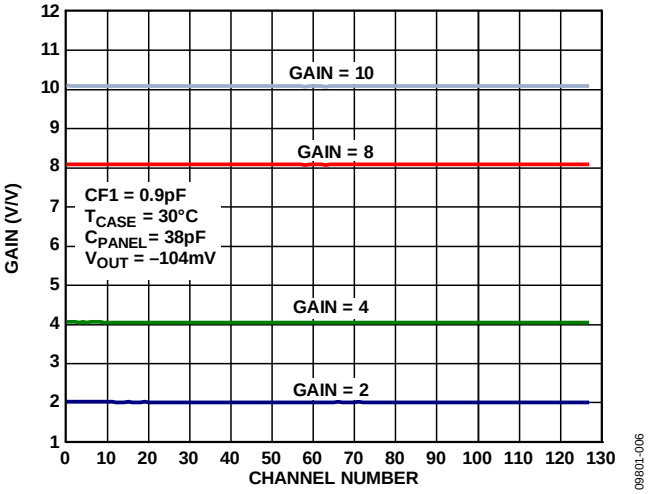


Figure 6. Gain vs. Channel for Four Values of Gain

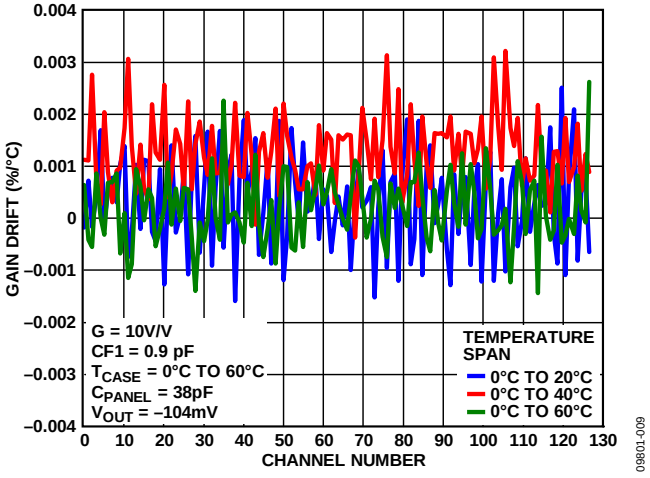


Figure 9. Gain Drift vs. Channel for Various Temperature Spans

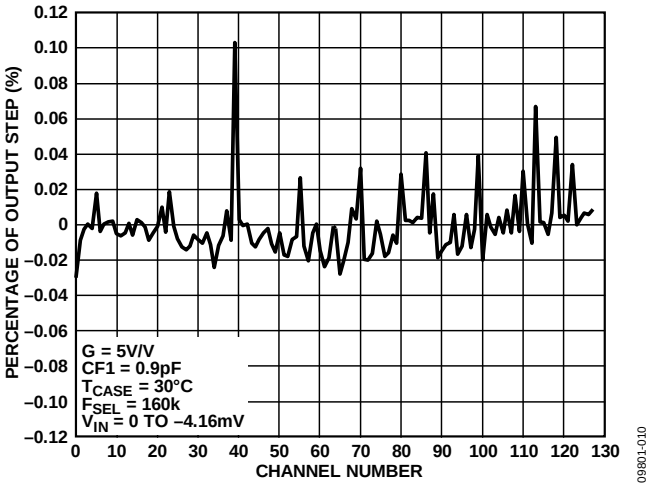


Figure 10. Adjacent Channel Crosstalk as Measured by the Percent of Output Step for Each Channel

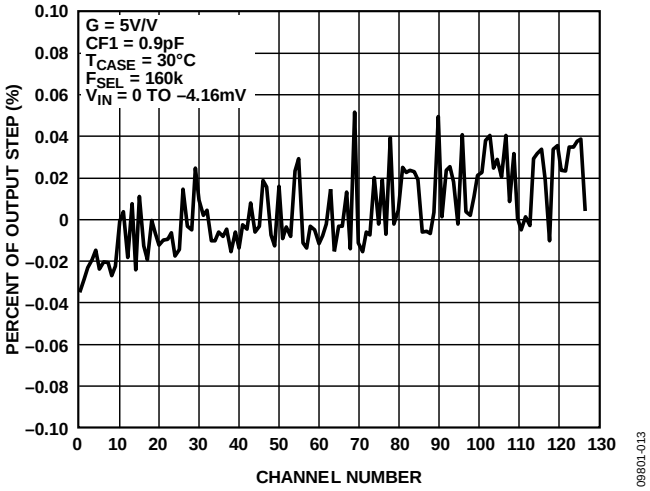


Figure 13. Crosstalk from All Nonadjacent Channels as Measured by the Percent of Output Step for Each Channel

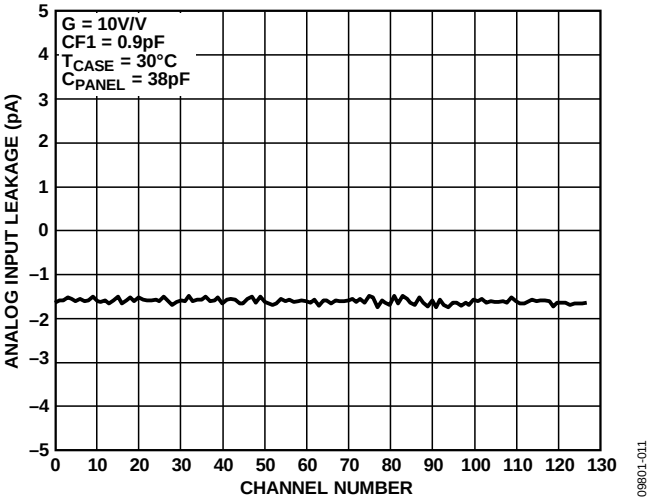


Figure 11. Input Leakage vs. Channel

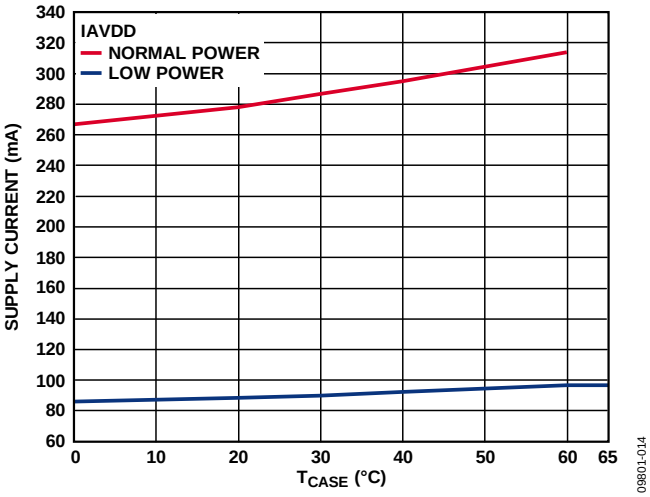


Figure 14. Supply Current vs. Temperature (T_{CASE})

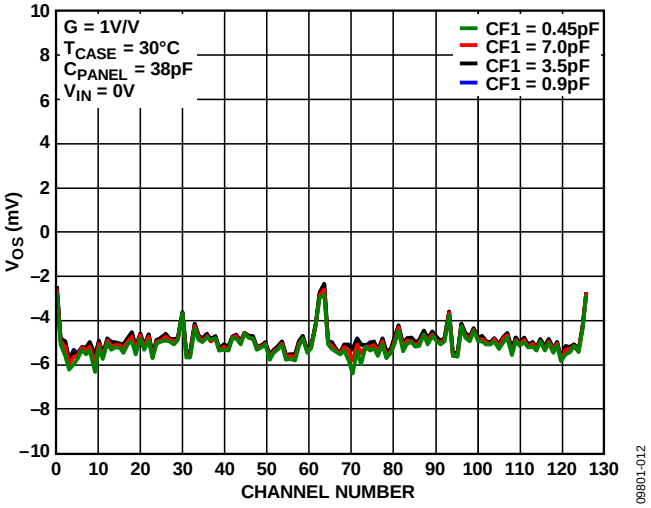


Figure 12. Differential Offset Voltage vs. Channel for Four Values of CF1

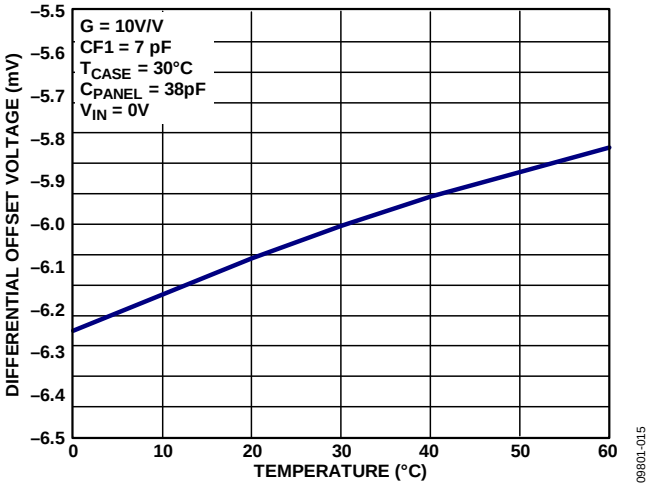


Figure 15. Differential Offset Voltage vs. Temperature

THEORY OF OPERATION

OVERVIEW

The AD8488 is a 128-channel AFE intended for interfacing thin film transistor (TFT) detector panel arrays in various digital X-ray applications (see Figure 1). The device includes a 128 dual stage, charge conversion amplifiers, internal timing, and control circuitry, a 128:1 differential output multiplexer, and an analog output buffer. Only the detector panel and a minimal amount of analog circuitry are required to complete a 128-channel analog X-ray interface. The AD8488 AFE is packaged in a compact, 17 mm × 17 mm, 255-lead BGA.

Analog Amplifier

The AD8488 analog inputs are suitable for ac or dc connection to 128 X-ray detector panel outputs. The analog amplifier consists of two stages: an integrator followed by a correlated double sampling gain amplifier. Figure 16 is a simplified block diagram showing the basic elements of an analog channel.

The characteristic CMOS high gate impedance of the integrator minimizes source loading. Prior to sampling a gate line, all 128 mux analog channels are initialized with $\overline{RST}$, as shown in Figure 17. During the 6.1 µs GRST period, the gain amplifier acquires the reference level (2.048 V) and any low frequency ambient noise. Just prior to gate sampling, both op amps are unlocked and the feedback capacitors, CF1 and CF2, are connected. When a TFT gate line is activated (reference the bottom signal, TFT_GATE, in Figure 17), the charge of each detector cell is applied simultaneously to all 128 MOSFET integrator circuits, which begin to ramp over a 12 µs interval. As seen in Figure 16, the op amps are biased at the reference voltage, plus offset and low frequency noise error voltages. Together, the resultant differential output voltage comprises the CDS or correlated double sampled composite. Following the sampling period, the pixel charges are stored, and the charge is held for the next 133 clock cycles while the 128 channels are muxed and sampled sequentially. As the channels are selected in sequence, their outputs are applied to a dual channel, high precision, current feedback, high frequency op amp. The AD8488 was designed to drive an ADC such as the AD9244 differential input high speed converter.

The mux channels are enabled and selected by the timing inputs, CK_ENa and CK_ENb. These two signals gate the clock and internal counter that actually selects the mux channel. The multiplexers must be read sequentially as one interprets from the CK_ENa and CK_ENb lines in Figure 17. The read time for each channel is 1 clock cycle. The timing signals, GATED CLKa and GATED CLKb, are developed internally and are shown in Figure 17 for reference only.

Troubleshooting Channels

Using the TST_MODE enable pin, individual channels are accessible for troubleshooting. Referring to Table 8, the channel address follows two initialization words, 0x01 and 0x02, while the enable pin, TST_MODE, is asserted high.

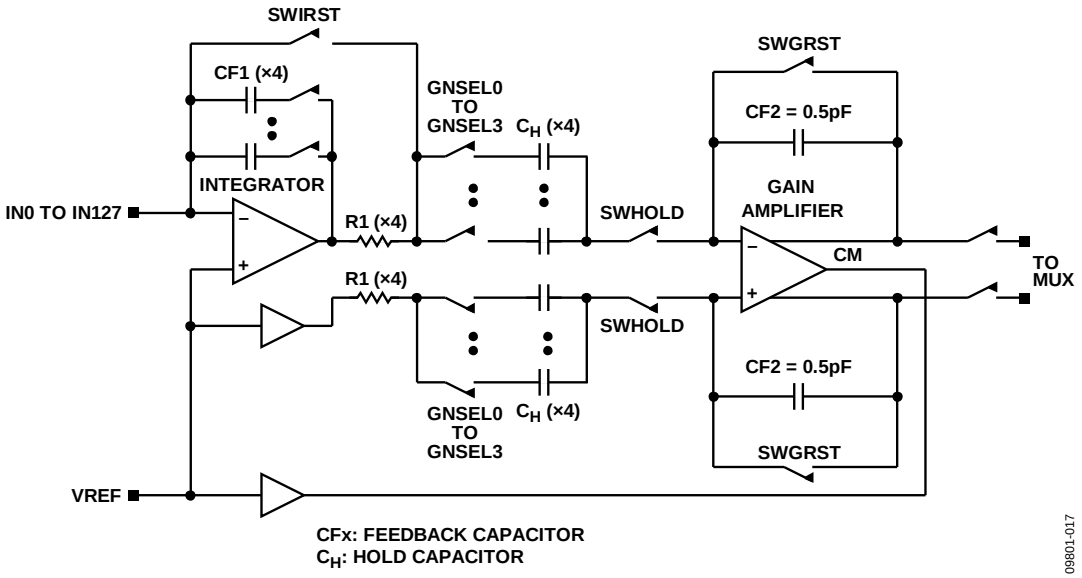


Figure 16. Block Diagram of an Integrator Channel

TIMING SIGNALS

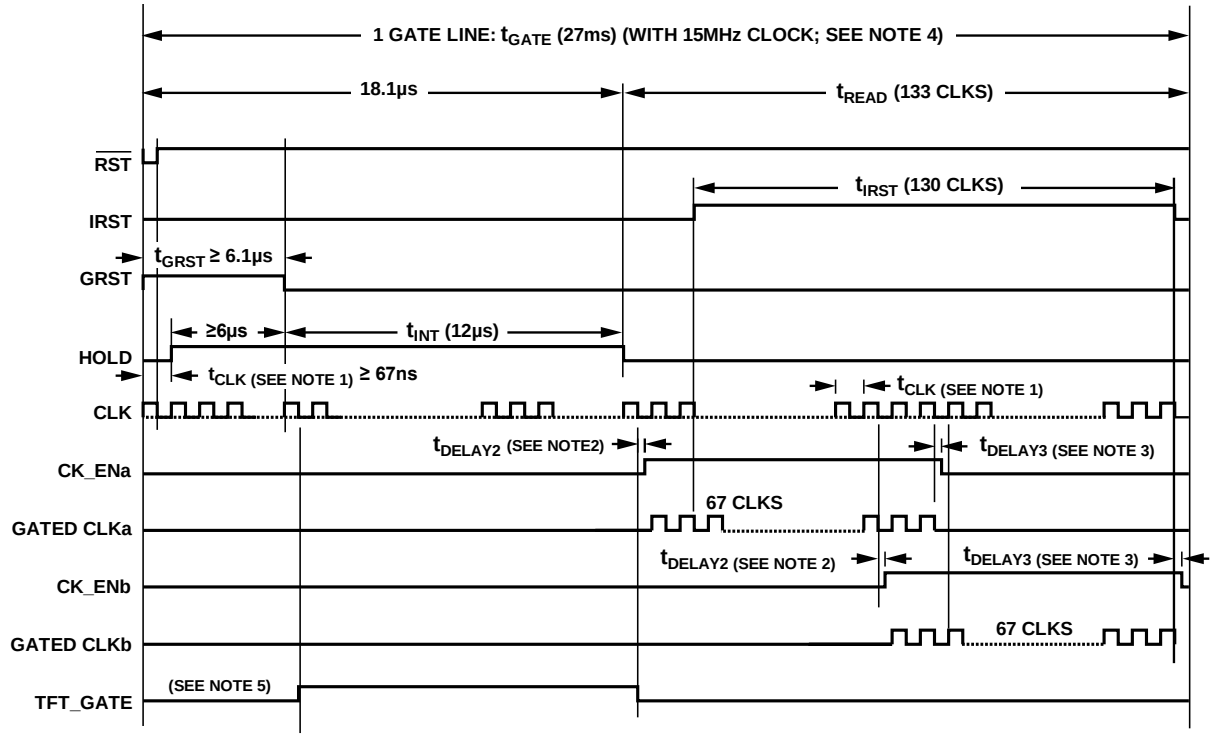
Figure 17 is the gate line timing diagram. The gate line sequence requires 405 clock cycles for channel integration and the sequential transfer to an ADC. The timing signals, IRST, GRST, and HOLD, control the integration, gain, and hold switches, respectively, and define the timing intervals required by each of the integrator channels. These signals may be generated by an FPGA, ROM, or similar device.

The balance of the signals shown in Figure 16 are user discretionary and encoded according to Table 8 through Table 11 for select gain, hold capacitor values, low-pass filter values, and mux output channels for troubleshooting.

Timing Notes

Refer to Figure 17 and the following timing notes:

1. The CLK frequency can range from 1 MHz to 15 MHz.
2. $\overline{RST}$ must be low (active) for the first half clock of the gate line cycle.
3. t_{GRST} must be ≥ 6.1 µs.
4. t_{INT} must be ≥ 12 µs.
5. The CK_ENa and CK_ENb intervals must be exactly 67 clocks. The time can be longer if t_{CLK} exceeds 67 ns.
6. The t_{IRST} interval must be exactly 130 CLKs.



NOTES
1. IN THIS EXAMPLE t_{CLK} = 67ns (15MHz).
2. ¼ CLK < t_{DELAY2} < ½ CLK.
3. 0 CLK < t_{DELAY3} < ¼ CLK.
4. $t_{GATE} = t_{GRST} + t_{INT} + t_{READ} = 27$µs.
5. ALL LOGIC LEVELS EXCEPT $\overline{RST}$ ARE ACTIVE HIGH.
6. SHOWN AS ACTIVE HIGH – CHARGE IS TRANSFERRED TO ALL CHANNELS DURING THIS INTERVAL.

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Figure 17. Gate Line Timing Diagram

APPLICATIONS INFORMATION

CONTROL REGISTER BIT MAPS

Table 8. Mux Switch Test Register Address Bits, Addresses Valid When TST = High

TST6	TST5	TST4	TST3	TST2	TST1	TST0	Selects Channel
0	0	0	0	0	0	0	None
0	0	0	0	0	0	1	−2
0	0	0	0	0	1	1	−1
0	0	0	0	0	1	0	0
0	0	0	0	1	1	0	1
0	0	0	0	1	1	1	2
0	0	0	0	1	0	1	3
0	0	0	0	1	0	0	4
0	0	0	1	1	0	0	5
0	0	0	1	1	0	1	6
0	0	0	1	1	1	1	7
0	0	0	1	1	1	0	8
0	0	0	1	0	1	0	9
0	0	0	1	0	1	1	10
0	0	0	1	0	0	1	11
0	0	0	1	0	0	0	12
0	0	1	1	0	0	0	13
0	0	1	1	0	0	1	14
0	0	1	1	0	1	1	15
0	0	1	1	0	1	0	16
0	0	1	1	1	1	0	17
0	0	1	1	1	1	1	18
0	0	1	1	1	0	71	19
0	0	1	1	1	0	0	20
0	0	1	0	1	0	0	21
0	0	1	0	1	0	1	22
0	0	1	0	1	1	1	23
0	0	1	0	1	1	0	24
0	0	1	0	0	1	0	25
0	0	1	0	0	1	1	26
0	0	1	0	0	0	1	27
0	0	1	0	0	0	0	28
0	1	1	0	0	0	0	29
0	1	1	0	0	0	1	30
0	1	1	0	0	1	1	31
0	1	1	0	0	1	0	32
0	1	1	0	1	1	0	33
0	1	1	0	1	1	1	34
0	1	1	0	1	0	1	35
0	1	1	0	1	0	0	36
0	1	1	1	1	0	0	37
0	1	1	1	1	0	1	38
0	1	1	1	1	1	1	39
0	1	1	1	1	1	0	40
0	1	1	1	0	1	0	41
0	1	1	1	0	1	1	42
0	1	1	1	0	0	1	43
0	1	1	1	0	0	0	44
0	1	0	1	0	0	0	45

TST6	TST5	TST4	TST3	TST2	TST1	TST0	Selects Channel
0	1	0	1	0	0	1	46
0	1	0	1	0	1	1	47
0	1	0	1	0	1	0	48
0	1	0	1	1	1	0	49
0	1	0	1	1	1	1	50
0	1	0	1	1	0	1	51
0	1	0	1	1	0	0	52
0	1	0	0	1	0	0	53
0	1	0	0	1	0	1	54
0	1	0	0	1	1	1	55
0	1	0	0	1	1	0	56
0	1	0	0	0	1	0	57
0	1	0	0	0	1	1	58
0	1	0	0	0	0	1	59
0	1	0	0	0	0	0	60
1	1	0	0	0	0	0	61
1	1	0	0	0	0	1	62
1	1	0	0	0	1	1	63

Table 9. Integrator Capacitor Content (CSEL0 and CSEL1)

CF1SEL1	CF1SEL0	CF1 (pF)
0	0	0.45
0	1	0.9
1	0	3.5
1	1	7.0

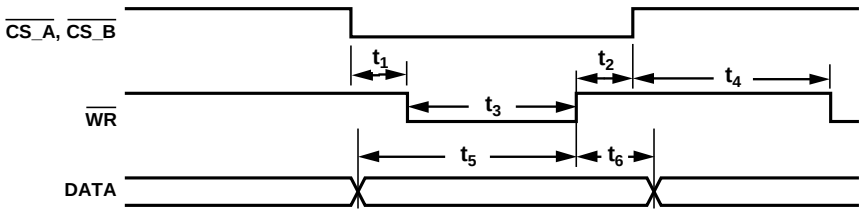
Table 10. Low-Pass Filter Time Constant—Resistor Selection Address Bits (FSEL0 and FSEL1)

FSEL1	FSEL0	R1 (kΩ)	Time Constant (µs)
0	0	195	1.5
0	1	130	1.0
1	0	65	0.5
1	1	0	0

Table 11. Gain Selection (Gain Amp/GNSEL0 to GNSEL3; CF2 = 0.5 pF)

GNSEL3 (CH3 = 1.5 pF)	GNSEL2 (CH2 = 2 pF)	GNSEL1 (CH = 1 pF)	GNSEL0 (CH = 0.5 pF)	Total CH (pF)	Gain
0	0	0	0	0	0
0	0	0	1	0.5	1
0	0	1	0	1	2
0	0	1	1	1.5	3
0	1	0	0	2	4
0	1	0	1	2.5	5
0	1	1	0	3	6
0	1	1	1	3.5	7
1	1	0	1	4	8
1	1	1	0	4.5	9
1	1	1	1	5	10

TIMING DIAGRAMS



NOTES
1. TIMING DIAGRAM TO WRITE A STATIC SIGNAL TO CHANNEL 0 TO CHANNEL 63 OR CHANNEL 64 TO CHANNEL127.
2. CS_A LOW OR CS_B LOW SELECTS CHANNEL 0 TO CHANNEL 63 OR CHANNEL 64 TO CHANNEL 127. WRITE DATA BY SEQUENCING WR LOW, THEN HIGH.

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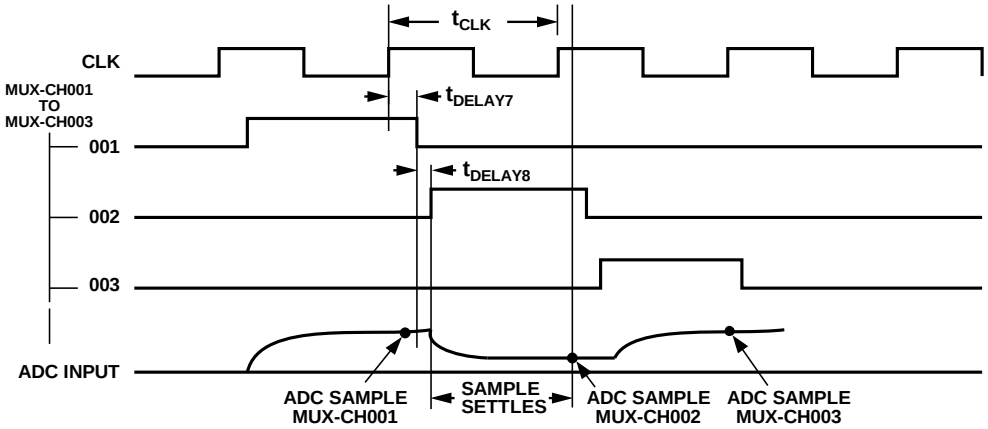
Figure 18. Input Register Timing Diagram



NOTES
1. ADC SAMPLES OCCUR WHEN MUX-CH001 TO MUX-CH003 IS HIGH, JUST PRIOR TO THE FALLING EDGE. SAMPLE MUST BE COMPLETE BEFORE HIGH TO LOW TRANSITION.

2. TIME DELAY SAMPLES (REFERENCE, INTERNAL ONLY):

	MIN.	TYP.	MAX.
t_{DELAY} 7:	5.3ns	6.6ns	7.8ns
t_{DELAY} 8:	1.2ns	1.4ns	1.7ns

3. t_A IS SYNCHRONOUS WITH ADC TIMING.

09801-020

Figure 19. Timing Diagram—AD8488 to ADC

OUTLINE DIMENSIONS

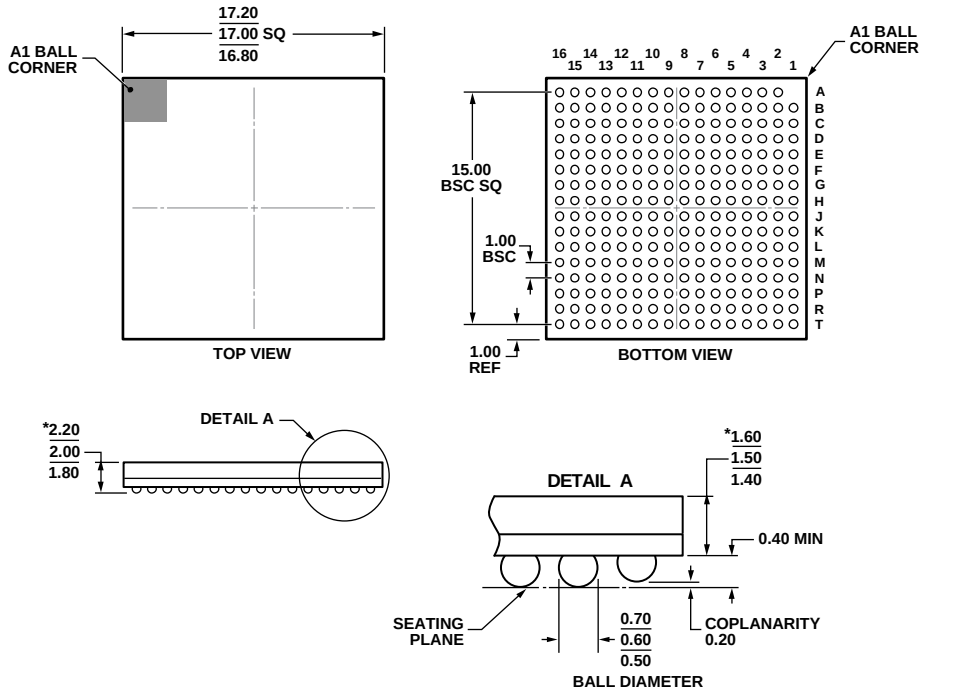


Figure 20. 255-Ball Chip-Scale Package Ball Grid Array [CSP_BGA]
(BC-255-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8488KBCZ	0°C to +85°C	255-Ball CSP_BGA	BC-255-1

[1] Z = RoHS Compliant Part.

NOTES

NOTES